REMARKS

Claims 2-7, 9-10, 12 and 15-19 are currently pending in this application. Claims 13 and 20 have been canceled. Claims 2, 9-10, 15 and 17 have been amended to more particularly point out and distinctly claim the invention. Support for the claim amendments can be found in the original claims, Figs. 2A and 3 and in the original Specification at paragraphs [0017]-[0021], among other places. Accordingly, no new matter has been added.

Entry of Amendment After Final

Applicants respectfully submit that: (1) no new matter has been added to the application by the amendment; (2) the amendment resolves all issues raised by the Examiner in the Office Action mailed August 25, 2004; (3) the subject matter of the amendment already has been included in the Examiner's search and therefore does not require the Examiner to perform further searching; and (4) the amendment places the application in condition for allowance or in better condition for appeal.

Consequently, Applicants respectfully request that the Amendment After Final Rejection be entered in accordance with 37 C.F.R. §116 and MPEP 714.13. In particular, entry of the Amendment herein is requested under 37 C.F.R. § 1.116 because such Amendment does not raise any new issues that would require further consideration and/or search since no change or *increase* in scope is being made to the scope of the proposed amended claims and new dependent claims therefrom. Claims 2, 9-10, 15 and 17 have been amended to more clearly recite the invention described and depicted in the original disclosure.

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 2-4 and 15-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,694,257 ("Klein *et al.*," hereinafter, "Klein"). The Examiner takes the position that Klein discloses a semiconductor device including an integrated circuit buffer that receives an input signal and generates a plurality of output signals that relate to the

input signal and an external resistor electrically connected to a delay generator, as well as other additional claimed features. The Examiner now clarifies that inherently a current I from V_{cc}/R_t goes "directly" to item 14, and therefore, affects the phase shift of the output of PLL, and that obviously current I varies as the resistance value of R_t varies which in turn influences the phase shift of output of PLL 18.

Withdrawal of the rejection of claims 2-4 and 15-19 is respectfully requested for at least the following reasons.

Present Invention

The present invention is directed to a semiconductor device having an integrated circuit buffer and a resistor. The buffer includes a delay generator. The buffer receives a clock input signal and generates a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal. The delay generator is configured to phase-shift the timing of the plurality of output signals with respect to the clock input signal. The resistor has a resistance value, a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference. The resistor is external to the integrated circuit buffer, and the resistance value determines a magnitude of the phase-shift caused by the delay generator.

Klein

Klein discloses a demodulation and data recovery circuit that demodulates a transmitted phase-coherent signal (i.e., a signal having data and clock intermixed) including recovery of clock and data signals. The circuit includes a clock recovery circuit having a one-shot 12 having both inverting and non-inverting inputs for receiving the phase-coherent modulated signal. The circuit also includes a resistor 20, which is connected between the one-shot 12 and a source of supply voltage. The circuit also includes a capacitor 22 which is connected between the one-shot 12 and a ground reference. The one-shot 12 is coupled to an input of a divide-by-two circuit 14, the output of which is coupled to an input terminal of a multiplexer 16. The multiplexer 16, for receiving a transmitted clock signal on a second input

terminal and for receiving an inverted silence signal, is coupled to a phase-locked loop (PLL) circuit 18. The phase-locked loop circuit 18 has an extracted clock output terminal, a two times clock output terminal and a four times clock output terminal. The one-shot 12 is used to recover the low frequency from the incoming signal. Every one-half bit time, another edge occurs which corresponds to the low frequency component. The output of the one-shot 12 is connected to the divide-by-two circuit 14 to obtain a square wave which is then fed to the phase-locked loop circuit 18 via the multiplexer 16. The multiplexer 16 is used to supply a frequency reference to the phase-locked loop circuit 18 and selects either the recovered clock signal or the transmitter clock signal (TXCLK) depending on whether there is in fact a valid signal being received. The data recovery circuit recovers the data by looking for an edge during a specific time window which is created using the extracted clock signal.

The one-shot, divide-by-two, multiplexer and PLL of Klein do not form a buffer circuit, as suggested by the Examiner. Instead, the Klein arrangement is for making edge triggered "windows" in order to recover "data." Additionally, the circuit of Klein does not receive a clock input and generate output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal. The outputs of Klein are not copies of the input, but rather separated components of the input for data, clock and then clock multiples.

Claim 2

Claim 2, recites, *inter alia*:

> an integrated circuit buffer having a delay generator, the buffer receiving a clock input signal and generating a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal, the delay generator being configured to phase-shift the timing of the plurality of output signals with respect to the clock input signal....

Klein fails to disclose or suggest a semiconductor that includes an integrated circuit buffer having a delay generator that is configured to generate a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal.

A claim is anticipated under 35 U.S.C. § 102 only if each and every element as set forth in the claim is found expressly or inherently described in a single prior art reference and the elements must be arranged as required in the claim. MPEP § 2131.

Klein discloses a demodulation and data recovery circuit that demodulates a transmitted phase-coherent signal (i.e., a signal having data and clock intermixed) including recovery of clock and data signals. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals.

The one-shot, divide-by-two, multiplexer and PLL of Klein do not form a buffer circuit, as suggested by the Examiner. Instead, the Klein arrangement is for making edge triggered "windows" in order to recover "data." Additionally, the circuit of Klein does not receive a clock input and generate output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal. The outputs of Klein are not copies of the input, but rather separated components of the input for data, clock and then clock multiples.

It is therefore, respectfully submitted, that independent claim 2 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 2. Claims 3-4 depend from claim 2. Accordingly, Applicants respectfully request that the rejection of independent claim 2 and dependent claims 3-4 under 35 U.S.C. § 102(b) be withdrawn.

Claim 15

Claim 15 recites, *inter alia*:

> receiving a clock input signal in the buffer;
> generating output signals from the buffer that are copies of the clock input signal delayed or advanced in time relative to the clock input signal; and
> phase-shifting the timing of one or more of the output signals with respect to the clock input signal in an amount that is dependent upon the resistance value of the external resistor.

Klein fails to disclose or suggest a method of adjusting the timing of an output signal of a semiconductor that includes connecting an external resistor to a buffer that generates a plurality of output signals which are copies of the clock input signal delayed or advanced in time relative to the clock input signal and phase-shifting the timing of one or more of the output signals with respect to the clock input signal in an amount that is dependent upon a resistance value of the external resistor.

As mentioned above, the one-shot, divide-by-two, multiplexer and PLL of Klein do not form a buffer circuit, as suggested by the Examiner. Instead, the Klein arrangement is for making edge triggered "windows" in order to recover "data." Additionally, the circuit of Klein does not receive a clock input and generate output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal. The outputs of Klein are not copies of the input, but rather separated components of the input for data, clock and then clock multiples.

It is therefore, respectfully submitted, that independent claim 15 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 15. Claim 16 depends from claim 15. Accordingly, Applicants respectfully request that the rejection of independent claim 15 and dependent claim 16 under 35 U.S.C. § 102(b) be withdrawn.

Claim 17

Claim 17 recites, *inter alia*:

> a buffer that receives the input signal from the input terminal which is configured to generate a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal and to phase-shift the timing of at least one of the plurality of output signals with respect to the clock input signal....

Klein fails to disclose or suggest a semiconductor that includes a buffer configured to generate a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal and to phase-shift the timing of at least one of the plurality of output signals with respect to the clock input signal.

As mentioned above, the one-shot, divide-by-two, multiplexer and PLL of Klein do not form a buffer circuit, as suggested by the Examiner. Instead, the Klein arrangement is for making edge triggered "windows" in order to recover "data." Additionally, the circuit of Klein does not receive a clock input and generate output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal. The outputs of Klein are not copies of the input, but rather separated components of the input for data, clock and then clock multiples.

It is therefore, respectfully submitted, that independent claim 17 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 17. Claims 18-20 depend from claim 17. Accordingly, Applicants respectfully request that the rejection of independent claim 17 and dependent claims 18-19 under 35 U.S.C. § 102(b) be withdrawn.

Claim 20

Claim 20 has been canceled, and therefore, the rejection under 35 U.S.C. § 102(b) with respect to claim 20 has been effectively rendered moot.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 6-7, 9-10 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of U.S. Patent No. 5,355,037 ("Andresen *et al.*," hereinafter, "Andresen"). The Examiner takes the position that Klein discloses all of the claimed limitations as recited in claim 1 (*sic.* – i.e., claim 2), but lacks a phased locked loop having a phase detector and a delay generator, a delay line and an external resistor that are electrically connected to adjust the timing. The Examiner takes the position that Andresen discloses a phased locked loop with a phase detector, a delay line and an internal feedback signal, and that it would have been obvious to modify the circuit of Klein to include the aforementioned features of Andresen.

Withdrawal of the rejection of claims 6-7, 9-10 and 12 is respectfully requested for at least the following reasons.

Andresen

Andresen discloses a phase-locked loop (PLL) circuit 10 which synchronizes a system clock signal with a chip clock signal of an individual integrated circuit. A system clock is input to a phase detector 11 and a delay path 13. The delay path 13 includes a digital delay line 15 and other delaying elements such as a high fanout clock distribution circuit 17. The clock distribution circuit 17 distributes the chip clock throughout the integrated circuit, and also feeds back the chip clock as an input to the phase detector 11. Because the system clock is provided at the input of delay path 13 and the chip clock is obtained at the output of delay path 13, the chip clock is time-shifted relative to the system clock due to the delay of the delay path 13.

Claims 6-7, 9-10 and 12

Claims 6-7, 9-10 and 12 depend upon independent claim 2.

In order to establish *prima facie* obviousness of a claimed invention, all the claimed limitations must be taught or suggested by the prior art. MPEP § 2143.03. Even further, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP § 2143.01. If the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. Id.

Klein fails to disclose, teach, or suggest a semiconductor that includes an integrated circuit buffer having a delay generator that receives a clock input signal and generates a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal, and the delay generator is configured to phase-shift the timing of the plurality of output signals with respect to the clock input signal, as claimed by all of claims 6-7, 9-10 and 12. Klein discloses a circuit that demodulates a transmitted phase-coherent signal including recovery of clock and data signals. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is

applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals.

Andresen merely discloses a phase-locked loop (PLL) circuit which synchronizes a system clock signal with a chip clock signal of an individual integrated circuit and a digital delay line.

Inserting the circuit of Andresen into the PLL of Klein, as suggested by the examiner would result in a confusing structure. If the output of the MUX of Klein were applied to the system clock line of Andresen, it is unclear how the data and clock would be demodulated – i.e., the thrust of Klein. Modifying the data demodulation circuit of Klein by the phase-locked loop (PLL) circuit of Andresen will therefore change the principle of operation of the Klein circuit and will likely result in a circuit that cannot demodulate data because the PLL of Andresen is expecting a clock signal not a mixed data signal.

The proposed combination suggested by the Examiner is a mere aggregation of components and would not result in a functioning device in accordance with the teachings of Klein or Andresen. Modifying Klein by Andresen would result in a device that does not function, and therefore, the proposed modification would render Klein unsatisfactory for its intended purpose. Thus, there is no motivation to make the proposed modification to Klein.

Thus, Klein modified by Andresen does not disclose all of the claimed features of claims 6-7, 9-10 and 12, as suggested by the Examiner. Therefore, claims 6-7, 9-10 and 12, are not *prima facie* obvious in view of Klein modified by Andresen. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of claims 6-7, 9-10 and 12 be withdrawn.

Claim 13

Claim 13 has been canceled, and therefore, the rejection under 35 U.S.C. § 103(a) with respect to claim 13 has been effectively rendered moot.

Allowable Subject Matter

The Examiner has stated that claim 5 is allowed.

CONCLUSION

In view of the foregoing Remarks , it is respectfully submitted that the present application, including claims 2-7, 9-10, 12 and 15-19, is in condition for allowance. Entry of the Rule 116 Amendment, withdrawal of the Final Rejection, and issuance of a Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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